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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/653,925	09/01/2000	Nikhil Vishwanath Kelkar	NSC1P181/P04767	7254

22434 7590 03/28/2003

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EXAMINER
PAREKH, NITIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/653,925	KELKAR ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE f this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-7,15-17,19-22,25 and 26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7,15-17,19-22,25 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

R quest for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 02/06/03 has been entered. An action on the RCE follows.

2. The amendment filed on 02/06/03 has been entered.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 5-7, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Frankeny et al. (US Pat. 5691041) in view of Akagawa et al. (US Pat. 5834844).

Regarding claim 1, Frankeny et al. disclose an integrated circuit (IC) package comprising:

- an IC die (1 in Fig. 6) having a top side and bottom side opposite to the top side, the top side of the die including raised interconnects/bumps (2 in Fig. 6) located over and conductively coupled to the die
- a solid flexible dielectric circuit film (FDCF)/interposer (3 in Fig. 6) having top and bottom surfaces, the FDCF being made of a plurality of layers (Col. 5, line 30) the FDCF having outer landing pads/plated layer and inner landing pads/plated layer being formed on the top/bottom surfaces respectively (not numerically referenced- see pads at locations 11, 12, 13, etc. and over interconnects 2 in Fig. 6; also see pads vias 6/7/8 in Fig. 2-4), the outer and inner landings/pads being fully supported by the circuit film, the outer and inner landings having a configuration such that the outer landing is being laterally offset from the inner landing (not numerically referenced- see outer pad at location 13 being connected to the inner pad under interconnect 2 in Fig. 6) or in alignment with the inner landing (not numerically referenced- see outer pad at location 11, 14, 18, etc. being connected to the inner pad under respective interconnects 2 in Fig. 6)
- the outer and inner landings being connected within the solid FDCF via a routing conductor/wiring layer (16 in Fig. 6) which extends laterally within the solid FDCF

- the FDCF being located over and conductively attached to the raised interconnects/bumps such that an air gap is formed between the IC die and the FDCF, and
- contact bumps/balls (9 in Fig. 6) being conductively coupled with the respective outer landings of the FDCF

(Fig. 6; Col. 4, line 30- Col. 6, line 65; Fig. 2-4).

Frankeny et al. fail to teach using at least one bond pad coupling the raised interconnect/bump on the topside of the die.

Akagawa et al. teach using an IC (32 in Fig. 22) having a variety of configurations of bonding pad/landings and an internal wiring where the under bump pads (60 in Fig. 22) are formed over the bonding pad/landing portions and being conductively coupled to the raised interconnects/projection bumps (Fig. 22 and 26-28; Col. 8, line 26-40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the top side of the die including at least one bond as taught by Akagawa et al. so that the bond strength and reliability can be improved in Frankeny et al's package.

Regarding claim 2, Frankeny et al. fail to specify the height of the air gap being in a range of 10-500 microns.

The determination of parameters such as air gap/spacing between the die and the substrate, bump height, bump/pad spacing/pitch/offset, size/dimension of the die/substrate, etc. in chip packaging and interconnection technology art is a subject of routing experimentation and optimization to achieve the overall package size, reliability and interconnection/repair/test requirements.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to select the air gap/height being in a range of 10-500 microns and incorporate the top side of the die including at least one bond as taught by Akagawa et al. so that the overall package size can be reduced and the reliability and interconnection/repair/test requirements can be improved in Frankeny et al's package.

Regarding claim 5, Frankeny et al. further teach using the spacing of the interconnects/bumps (2 and 9 in Fig. 6) being 250 microns such that the horizontal offset distance is in a range of 50-1000 microns (Col. 2, line 15).

Regarding claim 6, as explained above for claim 1, Frankeny et al. teach using the contact bumps (9 in Fig. 6) being conductively coupled with the respective outer landings of the FDCF.

Regarding claim 7, Frankeny et al. fail to teach using an under bump pad being formed over the bond pad and conductively coupling at least one bond pad and one raised interconnect.

Akagawa et al. teach using an IC (32 in Fig. 22) having a variety of configurations of bonding pad/landings and an internal wiring where the under bump pads (60 in Fig. 22) are formed over the bonding pad/landing portions and being conductively coupled to the raised interconnects/projection bumps (Fig. 22 and 26-28; Col. 8, line 26-40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate an under bump pad being formed over the bond pad and conductively coupling at least one bond pad and one raised interconnect.
As taught by Akagawa et al. so that the bond strength and reliability can be improved in Frankeny et al's package.

Regarding claim 21, as explained above for claim 1, Frankeny et al. teach using the FDCF being made of multiple layers (Col. 5, line 30).

Regarding claim 22, Frankeny et al. teach connecting the outer and inner landings via a routing connector such as a plated through hole (not numerically referenced- see plated through hole connector connecting 2 and 9 at location 13 2 in Fig. 6; Col. 4, line 42) in such a way as to form a cantilever-like structure.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Frankeny et al. (US Pat. 5691041) and Akagawa et al. (US Pat. 5834844) as applied to claim 1 above, and further in view of Wang et al. (US Pat. 6081026).

Regarding claim 3, Frankeny et al. and Akagawa et al. teach substantially the entire claimed structure as applied to claim 1 above, except using the FDCF being substantially of the same size as the IC die.

Wang et al. teach using an IC package having a flexible dielectric circuit film (FDCF 100 in Fig. 1) where an IC die (104 in Fig. 1) has substantially the same size as the FDCF.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the top side of the die including at least one bond as taught by Akagawa et al. and the flexible circuit film having substantially the same size

6. Claims 15-17, 19, 20, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Frankeny et al. (US Pat. 5691041) in view of Mizuno et al. (US Pat. 6077757) and Akagawa et al. (US Pat. 5834844).

Regarding claim 15, Frankeny et al. disclose an integrated circuit (IC) package comprising:

- an IC die (1 in Fig. 6) having a top side and bottom side opposite to the top side, the top side of the die including raised interconnects/bumps (2 in Fig. 6) located over and conductively coupled to the die
- a solid flexible dielectric circuit film (FDCF)/interposer (3 in Fig. 6) having top and bottom surfaces, the FDCF being made of a plurality of layers (Col. 5, line 30) the FDCF having outer landing pads/plated layer and inner landing pads/plated layer being formed on the top/bottom surfaces respectively (not numerically referenced- see pads at locations 11, 12, 13, etc. and over interconnects 2 in Fig. 6; also see pads vias 6/7/8 in Fig. 2-4), the outer and inner landings/pads being fully supported by the circuit film, the outer and inner landings having a configuration such that the outer landing is being laterally offset from the inner landing (not numerically referenced- see outer pad at location 13 being
- connected to the inner pad under interconnect 2 in Fig. 6) or in alignment with the inner landing (not numerically referenced- see outer pad at location 11, 14, 18, etc. being connected to the inner pad under respective interconnects 2 in Fig. 6)
- the outer and inner landings being connected within the solid FDCF via a routing conductor/wiring layer (16 in Fig. 6) which extends laterally within the solid FDCF

- the FDCF being located over and conductively attached to the raised interconnects/bumps such that an air gap is formed between the IC die and the FDCF, and
- contact bumps/balls (9 in Fig. 6) being conductively coupled with the respective outer landings of the FDCF

(Fig. 6; Col. 4, line 30- Col. 6, line 65; Fig. 2-4).

Frankeny et al. fail to teach using:

a) the IC package having an IC wafer comprising a plurality of IC dice, and

b) at least one bond pad coupling the raised interconnect on the topside of the die.

a) Mizuno et al. teach forming an IC wafer scale package (WSP) package using a wafer and an insulating substrate (1 and 5 respectively in Fig. 4A-4F), the wafer comprising a plurality of IC die and being singulated to form a plurality of IC die packages (Col. 3, line 40- Col. 4, line 5, line 10).

b) Akagawa et al. teach using an IC (32 in Fig. 22) having a variety of configurations of bonding pad/landings and an internal wiring where the under bump pads (60 in Fig. 22) are formed over the bonding pad/landing portions and being conductively coupled to the raised interconnects/projection bumps (Fig. 22 and 26-28; Col. 8, line 26-40).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the IC package having an IC wafer comprising a plurality of IC dice as taught by Mizuno et al. and the dice having bond pads coupling the raised interconnect on the top side of the wafer die as taught by Akagawa et al. so that the bond strength and reliability can be improved and the cycle time in wafer scale process can be improved in Frankeny et al's IC package.

Regarding claim 16, Frankeny et al. fail to specify the height of the air gap being in a range of 10-500 microns.

The determination of parameters such as air gap/spacing between the die and the substrate, bump height, bump/pad spacing/pitch/offset, size/dimension of the die/substrate, etc. in chip packaging and interconnection technology art is a subject of routing experimentation and optimization to achieve the overall package size, reliability and interconnection/repair/test requirements.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the air gap/height being in a range of 10-500 microns and incorporate the top side of the die including at least one bond as taught by Akagawa et al. so that the overall package size can be reduced and the reliability and interconnection/repair/test requirements can be improved in Frankeny et al's package.

Regarding claim 17, Frankeny et al. Mizuno et al. and Akagawa et al. teach substantially the entire claimed structure as applied to claim 15 above, including the wafer comprising a plurality of under bump pads being formed over the bond pad and conductively coupling the respective bond pads.

Regarding claim 19, Frankeny et al. further teach using the spacing of the interconnects/bumps (2 and 9 in Fig. 6) being 250 microns such that the horizontal offset distance is in a range of 50-1000 microns (Col. 2, line 15).

Regarding claim 20, Frankeny et al. teach using the contact bumps (9 in Fig. 6) being conductively coupled with the respective outer landings of the FDCF.

Regarding claim 25, as explained above for claim 15, Frankeny et al. teach using the FDCF being made of multiple layers (Col. 5, line 30).

Regarding claim 26, Frankeny et al. teach connecting the outer and inner landings via a routing connector such as a plated through hole (not numerically referenced- see plated through hole connector connecting 2 and 9 at location 13 2 in Fig. 6; Col. 4, line 42) in such a way as to form a cantilever-like structure.

Respons to Argum nts

7. Applicant's arguments with respect to claims 1-3, 5-7, 15-17, 19-22, 25 and 26 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Nitin Parekh

03-23-03

Tom Thomas

TOM THOMAS
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